Amendment Under 37 C.F.R. §1.116 08/533,207

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3	matrix on an entire surface of the wafer except for on scribe lines between the
4	semiconductor chips, each semiconductor chip of said semiconductor chips
5	including:
6	a first surface upon which said bump electrodes are formed;
7	[a second surface opposite said first surface;]
8 cont.	a periphery adjacent said scribe lines;
9	a plurality of chip electrodes formed [on said second surface] between
10	said first surface and said wafer along said periphery; and
11	a plurality of interconnection layers, each of said interconnection layers
12	including a first end connected to a bump electrode of said bump electrodes and
13	a second end connected to a corresponding chip electrode of said chip
14	electrodes,
15	each of said bump electrodes being located at a position other than over
16	said corresponding chip electrode.
1 .	(Amended) A semiconductor wafer [as in claim 10] including:
2	a plurality of chip sections defined thereon by scribe lines, each chip
³ C O	section having bump electrodes formed simultaneously thereon, the scribe lines
4	for separating the chip sections from each other without dividing bump
5	electrodes thereon, said chip section including:
6	a plurality of chip electrodes positioned on said chip section; and
7	a plurality of interconnection layers for electrically connecting said chip
8	electrodes and said bump electrodes.
9	said bump electrodes being located at positions other than over said chip

wherein each of said interconnection layers comprises an aluminum layer

and a plating on said aluminum layer, wherein said plating contacts one of said

bump electrodes and said aluminum layer contacts one of said chip electrodes.

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electrodes,